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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,013	11/25/2003	Jiong-Ping Lu	TI 35669	6979

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EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,013	LU ET AL.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,5-10,12 and 18* is/are rejected.

7)☒ Claim(s) *4 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claim 4 and 17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter: Prior art failed to teach or suggest the silicide lower capacitor electrode with surface roughness ranging from 1 nm to about 2 nm.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2, 3, 7-9, 13, 15 and 16 rejected under 35 U.S.C. 102(e) as being anticipated by Kim et at al. (2003/0058678).

Regarding Claim 2, Kim et al. disclose a ferroelectric memory device and method of fabricating the same where in Fig. 6 it is disclosed a recrystallized polysilicon layer 41 located over a gate electrode layer 13; and a capacitor located on said recrystallized polysilicon layer over said gate electrode layer, said capacitor, including; a first electrode 43 which comprises a

silicide; an insulator/ferroelectric layer 35 located over said first electrode 43; and a second electrode 37 located over said insulator/ferroelectric layer.

Regarding Claim 3, in paragraph 0017, cobalt silicide layer is disclosed.

Regarding Claim 7, in Fig. 6, Kim et al. disclose a semiconductor device, comprising: a recrystallized polysilicon layer 41 located over a gate electrode layer 13; and a capacitor located on said recrystallized polysilicon layer, said capacitor, including; a first electrode 43; an insulator/ferroelectric layer 35 located over said first electrode 43; and a second electrode 37 located over said insulator; wherein said gate electrode layer 13 is a polysilicon layer and said recrystallized polysilicon layer is located on said polysilicon.

Regarding Claim 8, polysilicon layer and said recrystallized polysilicon layer form at least a portion of a gate electrode stack 13.

Regarding Claim 9, in Figs 5-7 Kim et al. disclose forming an amorphous silicon layer 41 over a substrate 10, changing said amorphous silicon layer to a recrystallized polysilicon layer by subjecting said amorphous silicon layer to an annealing process, said annealing process causing said amorphous silicon layer to become said recrystallized polysilicon layer; and creating a capacitor on said recrystallized polysilicon layer, said capacitor including; a first electrode 41; an insulator/ferroelectric layer 35 located over said first electrode; a second electrode 37 located over said insulator

Regarding Claim 13, polysilicon layer and said recrystallized polysilicon layer form at least a portion of a gate electrode stack 13.

Regarding Claim 15, first electrode 41 comprises a silicide.

Regarding Claim 16, in paragraph 0017, cobalt silicide layer is disclosed

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et at al. (2003/0058678) in view of Voutsas et al. (6,642,092).

Regarding Claim 5, Kim et al. disclose a ferroelectric memory device and method of fabricating the same where in Fig. 6 it is disclosed a recrystallized polysilicon layer 41 located over a gate electrode layer 13; and a capacitor located on said recrystallized polysilicon layer over said gate electrode layer, said capacitor, including; a first electrode 43; an insulator/ferroelectric layer 35 located over said first electrode; and a second electrode 37 located over said insulator/ferroelectric layer, wherein said first electrode 41 comprises a silicide. Kim et al. fail to disclose the required thickness of the polysilicon layer. However, Voutsas et al. disclose a thin film transistor where in claim 27, a polysilicon layer of thickness between 10nm and 100 nm is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required polysilicon thickness in Kim et al. as taught by Voutsas et al. in order to have an optimum interface between the electrode layer and the polysilicon layer with the polysilicon layer having enough thickness and higher surface smoothness.

5. Claims 10, 12, 14 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et at al. (2003/0058678) as applied to claims 9 and 13 above, further in view of Voutsas et al. (6,642,092).

Regarding Claims 10, 12, 14 and 18, Kim et al. disclose forming an amorphous silicon layer 41 over a substrate 10, changing said amorphous silicon layer to a recrystallized polysilicon layer by subjecting said amorphous silicon layer to an annealing process, said annealing process causing said amorphous silicon layer to become said recrystallized polysilicon layer; and creating a capacitor on said recrystallized polysilicon layer, said capacitor including; a first electrode 41; an insulator/ferroelectric layer 35 located over said first electrode; a second electrode 37 located over said insulator. Kim et al. fail to disclose the required polysilicon thickness and the annealing temperature. However, Voutsas et al. disclose a thin-film transistor where in claim 23, the required annealing temperature for the polysilicon formation is disclosed. Furthermore, in claim 23, the required thickness for the polysilicon layer is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time of the invention was made to include the required polysilicon thickness and the required polysilicon annealing temperature in Kim et al. as taught by Voutsas et al. in order to have an optimum interface between the electrode layer and the polysilicon layer with the polysilicon layer having enough thickness and higher surface smoothness.

Regarding Claim 12, in claim 23 of Voutsas et al. the annealing temperature is between 1000-1100 degrees.

Regarding Claims 10, 14 and 18, in claim 27, Voutsas et disclose the required polysilicon layer thickness of 10-100 nm.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
April 25, 2007

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER